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EXAMINER	
DUONG, CHRISTINE T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,188	AOKI, KEISUKE	
	Examiner	Art Unit	
	CHRISTINE DUONG	2416	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

This is in response to the Applicant's arguments and amendments filed on 12 February 2008 in which claims 1-20 are currently pending.

Information Disclosure Statement

The references listed in the Information Disclosure Statement, filed on 12 February 2008, have been considered by the examiner (see attached PTO-1449 form or PTO/SB/08A and 08B forms).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 7, 11-13, 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Robinett et al. (PG Pub US 2002/0126711 A1).

Regarding claims **1 and 11**, Robinett et al. discloses a multiplexing apparatus which multiplexes a plurality of elementary data streams to generate one multiplexed stream (fig. 1), the multiplexing apparatus comprising:

a memory which stores a plurality of data units that are composed of an arbitrary amount of said elementary data streams ("The use of the cache 114 enables transport

packets to be received and stored or to be retrieved and outputted" [0074] lines 4-6 and further "TSs are bit streams that contain the data of one or more compressed/encoded audio-video programs. Each TS is formed as a sequence of fixed length transport packets" [0033] lines 4-7);

an instruction generating means for generating a plurality of multiplexing instruction data which describes a storage location of each data unit and storing the multiplexing instruction data into the memory in an order that said plurality of data units are to be multiplexed ("The cache 114 also stores descriptor data for each transport packet" [0074] lines 8-9 and "The DMA control circuit 116 can also obtain control of a sufficient number of descriptor storage locations, and the packet storage locations to which they point, in the cache 114. The DMA control circuit 116 obtains control of such descriptor and transport packet storage locations for the cache 114. This enables continuous allocation of descriptors and transport packet storage locations to incoming transport packets as they are received (i.e., from successive time slots)" [0076] lines 7-16); and

a multiplexed stream generating means for generating one multiplexed stream by reading the multiplexing instruction data sequentially from the memory and outputting the data unit corresponding to the multiplexing instruction ("combine program information of two TSs, namely, TS1 and TS2, into a third TS, namely, TS3" [0093] lines 5-7; "TS1 illustratively is received at a first adaptor 110, TS2 illustratively is received at a second adaptor 110 and TS3 illustratively is transmitted from a third adaptor 110 of the same remultiplexer node 100" [0093] lines 10-13; "the processor 160 examines

descriptors from the receipt queues (and/or possibly other queues containing descriptors of transport packets not yet scheduled for output) and identifies up to j≥1 descriptors pointing to transport packets to be outputted from the interrupting adaptor 110"; and further "The data link control circuit 112 sequentially retrieves from the cache 114 each descriptor in the transmit queue, in order from the head pointer 124-3, and the transport packet in the transport packet storage location to which the descriptor points" [0144] lines 1-5).

Regarding claims **2 and 12**, Robinett et al. discloses a multiplexing apparatus which multiplexes a plurality of elementary data streams to generate one multiplexed stream (fig. 1), the multiplexing apparatus comprising:

a memory which stores a plurality of data units that are composed of an arbitrary amount of said elementary data streams ("The use of the cache 114 enables transport packets to be received and stored or to be retrieved and outputted" [0074] lines 4-6 and further "TSs are bit streams that contain the data of one or more compressed/encoded audio-video programs. Each TS is formed as a sequence of fixed length transport packets" [0033] lines 4-7);

an instruction generating means for generating a plurality of multiplexing instruction data which describes a storage location of each data unit while generating command instruction data having stated therein an instruction for execution of a data processing to be executed in an arbitrary position in the multiplexing instruction data, and storing the multiplexing instruction data and command instruction data into the memory in an order that the plurality of data units and execution instruction are to be

multiplexed ("The cache 114 also stores descriptor data for each transport packet" [0074] lines 8-9; and "The DMA control circuit 116 can also obtain control of a sufficient number of descriptor storage locations, and the packet storage locations to which they point, in the cache 114. The DMA control circuit 116 obtains control of such descriptor and transport packet storage locations for the cache 114. This enables continuous allocation of descriptors and transport packet storage locations to incoming transport packets as they are received (i.e., from successive time slots)" [0076] lines 7-16; and "each receipt descriptor has a field 129-9 in which information pertinent to scrambling or descrambling can be stored, such as the control word to be used in scrambling the transport packet or a pointer to the appropriate control word table containing control words for use in scrambling or descrambling the transport packet" [0165] lines 3-9);

a multiplexed stream generating means for generating one multiplexed stream including the elementary data streams and command data by reading the multiplexing instruction data and command instruction data sequentially from the memory and outputting the data unit corresponding to the multiplexing instruction data, after reading the multiplexing instruction data ("combine program information of two TSs, namely, TS1 and TS2, into a third TS, namely, TS3" [0093] lines 5-7; "TS1 illustratively is received at a first adaptor 110, TS2 illustratively is received at a second adaptor 110 and TS3 illustratively is transmitted from a third adaptor 110 of the same remultiplexer node 100" [0093] lines 10-13; "the processor 160 examines descriptors from the receipt queues (and/or possibly other queues containing descriptors of transport packets not yet scheduled for output) and identifies up to $j \geq 1$ descriptors pointing to transport

packets to be outputted from the interrupting adaptor 110"; and further "The data link control circuit 112 sequentially retrieves from the cache 114 each descriptor in the transmit queue, in order from the head pointer 124-3, and the transport packet in the transport packet storage location to which the descriptor points" [0144] lines 1-5), or by outputting command data having stated therein the execution instruction stated in the command instruction data, after reading the command instruction data ("In processing descriptors and transport packets, the descrambler 115 uses the PID of the transport packet, to which the currently examined descriptor points, to index a descrambling map located in the cache 114" [0172] lines 1-4 and "The indexed entry of the descrambling map indicates whether or not the transport packet is scrambled and, if scrambled, one or more control words that can be used to descramble the transport packet. The indexed entry of the descrambling map can contain the control words corresponding to the PID of the transport packet or a pointer to a memory location in which the respective control word is stored" [0172] lines 11-18); and

a command executing means which is supplied with a multiplexed stream output from the multiplexed stream generating means and makes a processing corresponding to an instruction content stated in the command data when a data row in the multiplexed stream is command data ("If the indexed entry of the descrambling map indicates that the transport packet is to be descrambled, the descrambler 115 obtains the control word corresponding to the PID of the transport packet and descrambles the transport packet data using the control word" [0172] lines 1-5), or outputs the multiplexed stream as it is when the data row in the input multiplexed stream is elementary data stream ("If the

indexed entry of the descrambling map indicates that the transport packet to which the accessed descriptor points is not to be descrambled, the descrambler 115 simply sets the status bit(s) 129-7 of the descriptor to indicate that the next processing step, according to the order of the defined sequence of processing steps, may be performed on the descriptor and transport packet to which it points" [0172] lines 18-25).

Regarding claims **3 and 13**, Robinett et al. discloses everything claimed as applied above (see claims 2 and 12, respectively). In addition, Robinett et al. discloses the multiplexed stream generating means outputs, synchronously with the multiplexed stream, an ID flag for identifying which data row in the multiplexed stream is command data or elementary data stream ("each receipt descriptor has a field 129-9 in which information pertinent to scrambling or descrambling can be stored, such as the control word to be used in scrambling the transport packet or a pointer to the appropriate control word table containing control words for use in scrambling or descrambling the transport packet" [0165] lines 3-9);

the command executing means judges based on the ID flag whether the data row in the multiplexed stream is command data or elementary data stream ("In processing descriptors and transport packets, the descrambler 115 uses the PID of the transport packet, to which the currently examined descriptor points, to index a descrambling map located in the cache 114" [0172] lines 1-4 and "If the indexed entry of the descrambling map indicates that the transport packet to which the accessed descriptor points is not to be descrambled, the descrambler 115 simply sets the status bit(s) 129-7 of the descriptor to indicate that the next processing step, according to the order of the defined

sequence of processing steps, may be performed on the descriptor and transport packet to which it points. If the indexed entry of the descrambling map indicates that the transport packet is to be descrambled, the descrambler 115 obtains the control word corresponding to the PID of the transport packet and descrambles the transport packet data using the control word" [0172] lines 18-25 and [0173] lines 1-5).

Regarding claims **7 and 17**, Robinett et al. discloses everything claimed as applied above (see claims 2 and 12, respectively). In addition, Robinett et al. discloses the instruction generating means generates, when sending a timing acknowledgment in an arbitrary timing in an output multiplexed stream, command instruction data having stated therein an instruction for sending a timing acknowledgment ("The field 129-5 is for storing the receipt time for an incoming received transport packet or for storing the dispatch time of an outgoing to-be-transmitted transport packet" [0086]);

the multiplexed stream generating means outputs, when the command instruction data has stated therein an instruction for sending the timing acknowledgment, the command data having stated therein the content stated in the command instruction data ("The actual dispatch time is then stored in field 129-5 of the transmit descriptor. As described below, the actual dispatch time is really an approximate time at which the data link control circuit 112 of the third adaptor 110 (which outputs the remultiplexed TS TS3) submits the corresponding transport packet for output" [0138] lines 31-35); and

the command executing means sends, when the command data has stated therein an instruction for sending the timing acknowledgment, the timing

acknowledgment in a position of the command data in the multiplexed stream ("When the time of the reference clock generator 113 of the third adaptor 110 equals the time indicated in the dispatch time field 129-5 of the retrieved descriptor, the data link control circuit 112 transmits the transport packet, to which the descriptor (in the storage location pointed to by the head pointer 124-3) points, in TS3" [0144] lines 5-10).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-6 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinett et al. further in view of Kelly et al. (PG Pub US 2001/0036355 A1).

Regarding claims **4 and 14**, Robinett et al. discloses everything claimed as applied above (see claims 2 and 12, respectively). However, although Robinett et al. discloses "remultiplexing involves the selective modification of the content of a TS, such as adding transport packets to a TS" ([0025] lines 1-3), Robinett et al. fails to specifically disclose the instruction generating means generates, when inserting stuffing data into an output multiplexed stream, command instruction data having stated therein an instruction for inserting the stuffing data and an amount of the stuffing data; the multiplexed stream generating means outputs, when the command instruction data has stated therein an instruction for inserting the stuffing data, the command data having stated therein the content stated in the command instruction data; and the command

executing means inserts, when the command data has stated therein an instruction for inserting the stuffing data, stuffing data whose amount is stated in the command data to a position of the command data in the multiplexed stream.

Nevertheless, Kelly et al. teaches "depending on the contents of field AFC, there may be present an adaptation field AF, occupying some of the space otherwise allocated to payload data. The adaptation field AF may for example contain a discontinuity indicator flag as defined in ISO/IEC 13818 for MPEG2. When set to `1`, this flag indicates that the discontinuity state is true for the current Transport Stream packet. The discontinuity indicator is used to indicate two types of discontinuities, system time-base discontinuities and continuity counter discontinuities. In addition to optional data fields of pre-defined meaning, the adaptation field can be padded with stuffing bytes, so as to match the PES packet ends to TS packet boundaries" (Kelly et al. [0061]) and "stuffing can be done by either adding a PES stuffing packet or by adding an adaptation field. The adaptation field allows any desired number of data bytes to be added to the PES packet, as described in the MPEG specification. The data can be meaningless for stuffing purposes" (Kelly et al. [0122] lines 12-17).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to generate in the instruction generating means, when inserting stuffing data into an output multiplexed stream, command instruction data having stated therein an instruction for inserting the stuffing data and an amount of the stuffing data; output in the multiplexed stream generating means, when the command instruction data has stated therein an instruction for inserting the stuffing

data, the command data having stated therein the content stated in the command instruction data; and insert in the command executing means, when the command data has stated therein an instruction for inserting the stuffing data, stuffing data whose amount is stated in the command data to a position of the command data in the multiplexed stream because "audio frames are not aligned with Transport packets, it may be necessary to stuff part of the last audio packet to remove the start of the next audio frame" (Kelly et al. [0122] lines 9-12).

Regarding claims **5 and 15,** Robinett et al. discloses everything claimed as applied above (see claims 2 and 12, respectively). However, although Robinett et al. discloses "remultiplexing involves the selective modification of the content of a TS, such as deleting transport packets from a TS" ([0025] lines 1-4), Robinett et al. fails to specifically disclose the instruction generating means generates, when deleting data from an output multiplexed stream, command instruction data having stated therein a data delete instruction and data amount to be deleted; the multiplexed stream generating means outputs, when the command instruction data has stated therein an instruction for deletion of data, the command data having stated therein the content stated in the command instruction data; and the command executing means deletes, when the command data has stated therein an instruction for deletion of the data, an amount of data stated in the command data from a multiplexed stream next to the command data.

Nevertheless, Kelly et al. teaches "To avoid problems with the audio buffer model, it may be necessary to delete some audio packets. After the end of the last

video frame in the first stream SEQ1, once the start of a new audio frame is found, that packet and all subsequent audio packets should be deleted before sending over the digital interface. Conventional null TS packets can be inserted in their place, to preserve the TS format. Leading audio (i.e. audio that precedes the first video packet) is deleted similarly to avoid problems with audio buffer overflow" (Kelly et al. [0157]).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to generate in the instruction generating means, when deleting data from an output multiplexed stream, command instruction data having stated therein a data delete instruction and data amount to be deleted; output in the multiplexed stream generating means, when the command instruction data has stated therein an instruction for deletion of data, the command data having stated therein the content stated in the command instruction data; and delete in the command executing means, when the command data has stated therein an instruction for deletion of the data, an amount of data stated in the command data from a multiplexed stream next to the command data because "the null packets may be deleted by re-multiplexing processes and, therefore, the delivery of the payload of null packets to the decoder cannot be assumed" (Kelly et al. [0138] lines 5-8).

Regarding claims **6 and 16**, Robinett et al. discloses everything claimed as applied above (see claims 2 and 12, respectively). However, although Robinett et al. discloses "remultiplexing involves the selective modification of the content of a TS, such as adding transport packets to a TS" ([0025] lines 1-3), Robinett et al. fails to specifically disclose the instruction generating means generates, when inserting arbitrary data into

an output multiplexed stream, command instruction data having stated therein an instruction for insertion of the arbitrary data; the multiplexed stream generating means outputs, when the command instruction data has stated therein an instruction for insertion of the arbitrary data, the command data having stated therein the content stated in the command instruction data; and the command executing means inserts, when the command data has stated therein an instruction for insertion of the arbitrary data, the arbitrary data stated in the command data to a position of the command data in the multiplexed stream.

Nevertheless, Kelly et al. teaches "depending on the contents of field AFC, there may be present an adaptation field AF, occupying some of the space otherwise allocated to payload data. The adaptation field AF may for example contain a discontinuity indicator flag as defined in ISO/IEC 13818 for MPEG2. When set to `1`, this flag indicates that the discontinuity state is true for the current Transport Stream packet. The discontinuity indicator is used to indicate two types of discontinuities, system time-base discontinuities and continuity counter discontinuities. In addition to optional data fields of pre-defined meaning, the adaptation field can be padded with stuffing bytes, so as to match the PES packet ends to TS packet boundaries" (Kelly et al. [0061]) and "stuffing can be done by either adding a PES stuffing packet or by adding an adaptation field. The adaptation field allows any desired number of data bytes to be added to the PES packet, as described in the MPEG specification. The data can be meaningless for stuffing purposes" (Kelly et al. [0122] lines 12-17).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to generate in the instruction generating means, when inserting arbitrary data into an output multiplexed stream, command instruction data having stated therein an instruction for insertion of the arbitrary data; output in the multiplexed stream generating means, when the command instruction data has stated therein an instruction for insertion of the arbitrary data, the command data having stated therein the content stated in the command instruction data; and insert in the command executing means, when the command data has stated therein an instruction for insertion of the arbitrary data, the arbitrary data stated in the command data to a position of the command data in the multiplexed stream because "audio frames are not aligned with Transport packets, it may be necessary to stuff part of the last audio packet to remove the start of the next audio frame" (Kelly et al. [0122] lines 9-12).

5. Claims 8-9 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinett et al. further in view of Dobson et al. (US Patent No. 6,188,703 B1).

Regarding claims **8 and 18**, Robinett et al. discloses a multiplexing apparatus which multiplexes a plurality of elementary data streams to generate one multiplexed stream (fig. 1), the multiplexing apparatus comprising:

a memory which stores a plurality of data units that are composed of an arbitrary amount of said elementary data streams ("The use of the cache 114 enables transport packets to be received and stored or to be retrieved and outputted" [0074] lines 4-6 and further "TSs are bit streams that contain the data of one or more compressed/encoded

audio-video programs. Each TS is formed as a sequence of fixed length transport packets" [0033] lines 4-7);

a counting means for indicating a count which indicates a data occupancy of the memory ("A queue is implemented in each ring 124 by designating a pointer 124-3 to a head of the queue or first used/allocated descriptor storage location 129 in the queue and a pointer 124-4 to a tail of the queue or last used/allocated descriptor storage location 129 in the queue" [0081] lines 1-5);

an instruction generating means for generating a plurality of multiplexing instruction data which describes a storage location of each data unit and storing the multiplexing instruction data into the memory in an order that said plurality of data units are to be multiplexed ("The cache 114 also stores descriptor data for each transport packet" [0074] lines 8-9 and "The DMA control circuit 116 can also obtain control of a sufficient number of descriptor storage locations, and the packet storage locations to which they point, in the cache 114. The DMA control circuit 116 obtains control of such descriptor and transport packet storage locations for the cache 114. This enables continuous allocation of descriptors and transport packet storage locations to incoming transport packets as they are received (i.e., from successive time slots)" [0076] lines 7-16); and

a multiplexed stream generating means for generating one multiplexed stream by reading the multiplexing instruction data sequentially from the memory and outputting the data unit corresponding to the multiplexing instruction data ("combine program information of two TSs, namely, TS1 and TS2, into a third TS, namely, TS3" [0093] lines

5-7; "TS1 illustratively is received at a first adaptor 110, TS2 illustratively is received at a second adaptor 110 and TS3 illustratively is transmitted from a third adaptor 110 of the same remultiplexer node 100" [0093] lines 10-13; "the processor 160 examines descriptors from the receipt queues (and/or possibly other queues containing descriptors of transport packets not yet scheduled for output) and identifies up to j≥1 descriptors pointing to transport packets to be outputted from the interrupting adaptor 110"; and further "The data link control circuit 112 sequentially retrieves from the cache 114 each descriptor in the transmit queue, in order from the head pointer 124-3, and the transport packet in the transport packet storage location to which the descriptor points" [0144] lines 1-5);

the instruction generating means adding a data amount of a data unit corresponding to the multiplexing instruction data to the count ("The field 129-8 contains a transfer count indicating the number of bytes in a received incoming transport packet" [0089] and further "the field 129-3 is for storing the number of bytes of a to-be-outputted, outgoing transport packet" [0084] lines 1-2).

However, Robinett et al. fails to specifically disclose that the instruction generating means adds a data amount of a data unit corresponding to the multiplexing instruction data to the count and the counting means subtracts the data amount of output data unit from the count.

Nevertheless, Dobson et al. teaches "a video FIFO fullness counter 40 (see FIG. 4) then keeps track of the number of bytes of video data in the FIFO 32 at any time" (Dobson et al. column 4 lines 3-6) and "when a start code is detected, the value in the

FIFO-fullness-counter 40 is latched into another counter called the start-code position counter 48. The start-code position counter 48 only counts down on compressed data FIFO reads by the mux 30" (Dobson et al. column 4 lines 31-35).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to add a data amount of a data unit corresponding to the multiplexing instruction data to the count and subtract the data amount of output data unit from the count because "a count of the start-of-frame can be used to determine when to insert the PTS" (Dobson et al. column 5 lines 27-29).

Regarding claims **9 and 19**, Robinett et al. and Dobson et al. discloses everything claimed as applied above (see claims 8 and 18, respectively). However, Robinett et al. fails to disclose that the memory is divided into a plurality of storage areas correspondingly to the types of the elementary data streams and the elementary data streams is stored into corresponding storage areas; the counting means holds a plurality of counts corresponding to the storage areas in the memory; the instruction generating means adds the data amount of a data unit corresponding to the multiplexing instruction data to a count corresponding to a storage area in which the data unit is stored; and the counting means subtracts the data amount of data unit output from the memory from a count corresponding to the storage area in which the data unit is stored.

Nevertheless, Dobson et al. teaches "a video FIFO fullness counter 40 (see FIG. 4) then keeps track of the number of bytes of video data in the FIFO 32 at any time" (Dobson et al. column 4 lines 3-6) and "when a start code is detected, the value in the FIFO-fullness-counter 40 is latched into another counter called the start-code position

counter 48. The start-code position counter 48 only counts down on compressed data FIFO reads by the mux 30" (Dobson et al. column 4 lines 31-35) and "the audio mux logic circuit 18 performs similar functions to the video mux logic circuit 16. It buffers the audio elementary stream data, signals the mux processor 22 when there is sufficient audio data in the FIFO to form the payload of a MPEG-2 transport packet and signals the mux processor 22 when the data in the current payload contains an audio start-of-frame. Audio logic is implemented in exactly the same way as the video logic and is implemented in the same logic block" (Dobson et al. column 4 lines 48-56).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to divide the memory into a plurality of storage areas correspondingly to the types of the elementary data streams and to store the elementary data streams into corresponding storage areas; the counting means to hold a plurality of counts corresponding to the storage areas in the memory; the instruction generating means to add the data amount of a data unit corresponding to the multiplexing instruction data to a count corresponding to a storage area in which the data unit is stored; and the counting means to subtract the data amount of data unit output from the memory from a count corresponding to the storage area in which the data unit is stored because "a count of the start-of-frame can be used to determine when to insert the PTS" (Dobson et al. column 5 lines 27-29).

6. Claims 10 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robinett et al. further in view of Zaun et al. (PG Pub US 2001/0024456 A1).

Regarding claims **10 and 20**, Robinett et al. discloses a multiplexing apparatus which multiplexes a plurality of elementary data streams to generate a plurality of multiplexed streams (fig. 1), the multiplexing apparatus comprising:

a memory which stores a plurality of data units that are composed of arbitrary amounts of said elementary data streams ("The use of the cache 114 enables transport packets to be received and stored or to be retrieved and outputted" [0074] lines 4-6 and further "TSs are bit streams that contain the data of one or more compressed/encoded audio-video programs. Each TS is formed as a sequence of fixed length transport packets" [0033] lines 4-7);

an instruction generating means for generating a plurality of multiplexing instruction data which describe a storage location of each data unit and storing the multiplexing instruction data into the memory in an order that said plurality of data units are to be multiplexed ("The cache 114 also stores descriptor data for each transport packet" [0074] lines 8-9 and "The DMA control circuit 116 can also obtain control of a sufficient number of descriptor storage locations, and the packet storage locations to which they point, in the cache 114. The DMA control circuit 116 obtains control of such descriptor and transport packet storage locations for the cache 114. This enables continuous allocation of descriptors and transport packet storage locations to incoming transport packets as they are received (i.e., from successive time slots)" [0076] lines 7-16); and

a multiplexed stream generating means for generating a plurality of multiplexed streams by reading the multiplexing instruction data sequentially from the memory, and

outputting the data unit corresponding to the multiplexed instruction data ("one or more to-be-remultiplexed TSs, namely, TS1, TS2 and TS3, are received at the remultiplexer 30. As a result of the remultiplexing operation of the remultiplexer 30, one or more TSs, namely, TS4 and TS5, are outputted from the remultiplexer 30" [0065] lines 1-5; "the processor 160 examines descriptors from the receipt queues (and/or possibly other queues containing descriptors of transport packets not yet scheduled for output) and identifies up to j≥1 descriptors pointing to transport packets to be outputted from the interrupting adaptor 110"; and further "The data link control circuit 112 sequentially retrieves from the cache 114 each descriptor in the transmit queue, in order from the head pointer 124-3, and the transport packet in the transport packet storage location to which the descriptor points" [0144] lines 1-5)

the instruction generating means stating, in the multiplexing instruction data, the type of a multiplexed stream resulted from multiplexing data units corresponding to the generated multiplexing instruction data ("Each TS is provided with a four byte header that includes a packet identifier or "PID." The PID is analogous to a tag which uniquely indicates the contents of the transport packet. Thus, one PID is assigned to a video ES of a particular program, a second, different PID is assigned to the audio ES of a particular program, etc" [0018] lines 10-15).

However, Robinett et al. fails to specifically disclose the multiplexed stream generating means generating the plurality of multiplexed streams by switching the outputting of the data unit read correspondingly to the multiplexed stream type stated in the multiplexing instruction data.

Nevertheless, Zaun et al. teaches "the output processor 124 is a FPGA conducts the required hardware tasks to generate two or more output streams from the data stored in the packet buffers 104. More particularly, the output processor 124 reads the selected packet data from the input packet buffers and/or the insert packet buffer 112" (Zaun et al. [0035] lines 3-8) and "the output processing section then generates two or more independent high-speed transport multiplex (HSTM) output streams incorporating the selected packet data" (Zaun et al. [0035] lines 12-15) and "the bus control logic 400 responds to packet buffer interrupts, reads new packet information from the interrupting packet buffers, and generates addresses and chip selects to access data in the packet buffer as instructed by the output stream data registers. The chip selects in particular are used by the output processor 124 to read selected individual "chips" in the packet buffers 104" (Zaun et al. [0036] lines 3-9).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to generate the plurality of multiplexed streams by switching the outputting of the data unit read correspondingly to the multiplexed stream type stated in the multiplexing instruction data because "there are some applications where it is desirable to generate two or more output streams from the input streams" (Zaun et al. [0003] lines 5-6).

Response to Arguments

7. Applicant's arguments have been fully considered but they are not persuasive.

Applicants have argued regarding claim 1-3, 7, 11-13, 17 that "nothing in Robinett shows, teaches or suggests multiplexing a plurality of elementary data streams to generate one multiplexed stream" (page 3).

In response to Applicants' argument, the examiner respectfully disagrees. Robinett discloses "combine program information of two TSs, namely, TS1 and TS2, into a third TS, namely, TS3" [0093] lines 5-7; "TS1 illustratively is received at a first adaptor 110, TS2 illustratively is received at a second adaptor 110 and TS3 illustratively is transmitted from a third adaptor 110 of the same remultiplexer node 100" [0093] lines 10-13; "the processor 160 examines descriptors from the receipt queues (and/or possibly other queues containing descriptors of transport packets not yet scheduled for output) and identifies up to j≥1 descriptors pointing to transport packets to be outputted from the interrupting adaptor 110"; and further "The data link control circuit 112 sequentially retrieves from the cache 114 each descriptor in the transmit queue, in order from the head pointer 124-3, and the transport packet in the transport packet storage location to which the descriptor points" [0144] lines 1-5; and "constructing the outputted remultiplexed TS TS3 and dynamically constructing the remultiplexed TS TS3 from the content of the inputted to-be-remultiplexed TSs TS1 and TS2" [0094]. This shows that two data streams are multiplexed into one data stream. Therefore, Robinett discloses multiplexing a plurality of elementary data streams to generate one multiplexed stream.

Applicants have argued regarding claim 1-3, 7, 11-13, 17 that "nothing in Robinett shows, teaches or suggests generating the multiplexed stream by reading the

multiplexing instruction data sequentially from the memory and outputting the data units corresponding to the (read) multiplexing instruction data" (page 4).

In response to Applicants' argument, the examiner respectfully disagrees. Robinett discloses "The data link control circuit 112 sequentially retrieves from the cache 114 each descriptor in the transmit queue, in order from the head pointer 124-3, and the transport packet in the transport packet storage location to which the descriptor points" [0144] lines 1-5 and "The DMA control circuit 116 can maintain a sufficient number of transport packets (and descriptors therefor) in the cache 114 to enable the data link control circuit 112 to output transport packets in the output TS continuously (i.e., in successive time slots). The DMA control circuit 116 can also obtain control of a sufficient number of descriptor storage locations, and the packet storage locations to which they point, in the cache 114. The DMA control circuit 116 obtains control of such descriptor and transport packet storage locations for the cache 114. This enables continuous allocation of descriptors and transport packet storage locations to incoming transport packets as they are received (i.e., from successive time slots)" [0076]). This shows that the instruction data are read in order from memory and then outputted accordingly. Therefore, Robinett discloses generating the multiplexed stream by reading the multiplexing instruction data sequentially from the memory and outputting the data units corresponding to the (read) multiplexing instruction data.

Applicants have argued regarding claim 8-9, 18-19 that "nothing in Dobson shows, teaches, suggests multiplexing instruction data describing a storage location of each data unit" (pages 6-7).

In response to Applicants' argument, the examiner respectfully disagrees. As explained in the previous Office Action, Robinett discloses "The DMA control circuit 116 can also obtain control of a sufficient number of descriptor storage locations, and the packet storage locations to which they point, in the cache 114" [0076]. This shows that the data stream is stored in a specific location where a descriptor represents that location. Therefore, Robinett discloses multiplexing instruction data describing a storage location of each data unit.

Applicants have argued regarding claim 10, 20 that "nothing in Zaun shows, teaches or suggest generating a plurality of multiplexing instruction data, storing thereof and generating multiplexing streams by reading the multiplexing instruction data sequentially from a memory" (page 9).

In response to Applicants' argument, the examiner respectfully disagrees. As explained in the previous Office Action, Robinett discloses "The purpose of the cache 114 is to temporarily store the next one or more to-be-outputted transport packets pending output from the adaptor 110 or the last one or more transport packets recently received at the adaptor 110. The use of the cache 114 enables transport packets to be received and stored or to be retrieved and outputted with minimal latency (most notably without incurring transfer latency across the bus 130). The cache 114 also stores

descriptor data for each transport packet" [0074] and "The DMA control circuit 116 can maintain a sufficient number of transport packets (and descriptors therefor) in the cache 114 to enable the data link control circuit 112 to output transport packets in the output TS continuously (i.e., in successive time slots). The DMA control circuit 116 can also obtain control of a sufficient number of descriptor storage locations, and the packet storage locations to which they point, in the cache 114. The DMA control circuit 116 obtains control of such descriptor and transport packet storage locations for the cache 114. This enables continuous allocation of descriptors and transport packet storage locations to incoming transport packets as they are received (i.e., from successive time slots)" [0076]. This shows that data streams are received and a corresponding descriptor representing the data stream storage location is stored, which is later used to output. Therefore, Robinett discloses generating a plurality of multiplexing instruction data, storing thereof and generating multiplexing streams by reading the multiplexing instruction data sequentially from a memory.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTINE DUONG whose telephone number is (571)270-1664. The examiner can normally be reached on Monday - Friday: 830 AM-6 PM EST with second Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christine Duong/

Examiner, Art Unit 2416
11/12/2008

/Brenda Pham/

Primary Examiner, Art Unit 2416